REMARKS

Claims 1-20 were examined and reported in the Office Action. Claims 1-20 are rejected. Claims 1, 3, 4, 6-8, 11-13, and 18-19 are amended. Claims 1-20 remain. Applicant requests reconsideration of the application in view of the following remarks.

I. Double Patenting (non-statutory)

It is asserted in the Office Action that claim 1 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over respective Claims 1-4 of co-pending US Patent application No. 09/677,392. Applicant submits a terminal disclaimer in compliance with 37 CFR 3.73(b).

Accordingly, withdrawal of the double patenting rejection for claim 1 is respectfully requested.

II. 35 U.S.C. § 102(e)

It is asserted in the Office Action that claims 1-20 are rejected in the Office Action under 35 U.S.C. §102(e), as being unpatentable over U.S. Patent No. 6,181,151 B1, issued to Wasson ("Wasson"). Applicant respectfully disagrees.

According to MPEP 2131, "'[a] claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.' (Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987)). 'The identical invention must be shown in as complete detail as is contained in the ... claim.' (Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989)). The elements must be arranged as required by the claim, but this is not an ipsissimis verbis test, i.e., identity of terminology is not required. (In re Bond, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990))."

Applicant's amended claim 1 contains the limitations of "[a]n apparatus comprising: an internal test bus (ITB); a plurality of deskew clusters coupled to the ITB, wherein the plurality of deskew clusters each include a deskew controller; an integrated

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test controller (ITC) coupled to the ITB, said ITC having an instruction register and a test access port finite state machine (TAP FSM); and a debug unit coupled to the ITC; wherein the ITC generates a single global control signal and each of the deskew controllers generates a first local control signal and a second local control signal, where said ITC encodes and transmits states of said TAP FSM and test instructions to at least one logic unit controller over said ITB to test said apparatus."

Applicant's amended claim 6 contains the limitations of " [a] method comprising: generating a single global control signal in an integrated test controller within an integrated circuit; decoding the single global control signal in a deskew controller in the integrated circuit; generating a first local control signal corresponding to the single global control signal; distributing the first local control signal to a regional clock driver (RCD); and performing one of a debug operation and a testability operation on the integrated circuit by using the single global control signal and the first local control signal."

Applicant's amended claim 11 contains the limitations of "[a] program storage device readable by a machine comprising instructions that cause the machine to: generate a single global control signal in an integrated test controller within an integrated circuit; decode the single global control signal in a deskew controller within the integrated circuit; generate a first local control signal corresponding to the single global control signal; distribute the first local control signal to a regional clock driver (RCD); and perform one of a debug operation and a testability operation on the integrated circuit by using the single global control signal and the first local control signal."

Applicant's amended claim 16 contains the limitations of "[a] system comprising: at least one processor; a global bus coupled to the at least one processor; a memory coupled to the global bus; an internal test bus (ITB) located within the at least one processor; a plurality of deskew clusters coupled to the ITB, wherein the plurality of deskew clusters each include a deskew controller; an integrated test controller (ITC) coupled to the ITB; and a debug unit coupled to the ITC; wherein the ITC generates a

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single global control signal and each of the deskew controllers generates a first local control signal to test the at least processor."

Applicant's claimed invention tests and debugs a device (e.g., an integrated circuit) where the device, itself, contains all necessary components for carrying out the testing or debugging. The distributed test control scheme reduces the number of global test control lines, relaxes routing constraints on the test control lines, and adds greater flexibility in the physical placement of the test controller and test control logic.

Wasson discloses an integrated circuit (IC) tester. Wasson does not disclose, teach or suggest the IC tester is such that it is embedded on a device under test in order to be tested or debugged. The IC tester of Wasson is simply external to any device to be tested or debugged. Moreover, Wasson does not teach, disclose or suggest all the limitations contained in Applicant's amended claims 1, 6, 11 and 16, as listed above.

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Therefore, since Wasson does not disclose, teach or suggest all of Applicant's amended claims 1, 6, 11 and 16 limitations, Applicant respectfully asserts that a *prima facie* rejection under 35 U.S.C. § 102(b) has not been adequately set forth relative to Wasson. Thus, Applicant's amended claims 1, 6, 11 and 16 are not anticipated by Wasson. Additionally, the claims that directly or indirectly depend from claims 1, 10 and 18, namely claims 2-9, 11-17, and 19-20, respectively, would also not be obvious over Wasson for the same reason.

Accordingly, withdrawal of the 35 U.S.C. § 102(e), rejections for claims 1-20 are respectfully requested.

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CONCLUSION

In view of the foregoing, it is believed that all claims now pending, namely 1-20, patentably defines the subject invention over the prior art of record and are in condition for allowance and such action is earnestly solicited at the earliest possible date.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly extension of time fees.

Respectfully submitted,

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CERTIFICATE OF FACSIMILE TRANSMISSION

I hereby certify that this paper is being facsimile transmitted to the Patent and Trademark Office, Commissioner for Patents, Post Office Box 1450, Alexandria, Virginia 22313-1450, on November 25, 2003.

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